REMARKS/ARGUMENTS

Claims 13-24 and 26-43 remain pending in this application. Claims 6 through 12 were withdrawn in response to the Examiner's restriction requirement in the previous Office Action. Claims 1-5 and 25 have hereby been cancelled, without prejudice or disclaimer to the subject matter contained therein. New claims 31 through 43 have been added to the application. New claims 32 through 36 have been added in place of former claims 1 through 5 as it is believed that these claims better define the present invention and the scope of protection to which the applicant believes it is entitled. New claims 31 and 37 through 43 have been added to the application to capture the scope of protection to which the applicant believes it is entitled. The new claims have been added to improve the readability of the claims and not in response to any statutory requirements. New claims 32 through 36 do not narrow the scope of protection claimed in former claims 1 through 5 and therefore do not constitute a narrowing amendment.

Claims 13, 14, 23, 24, and 26 have been amended as detailed-above to improve their readability. The amendments to claims 13, 14, 23, 24 and 26 have not narrowed the scope of protection defined by those claims.

Following entry of the foregoing amendments, there are 30 claims pending in the application, 5 of which are independent claims. The application was originally filed with 30 claims, 5 of which were independent claims. Accordingly, the applicant believes that no excess claim fees are due as a result of the foregoing amendments. If necessary, the Commissioner is hereby authorized to charge any fees, including excess claim fees, and any overpayments to deposit account No. 13-2400 in this, concurrent, and future replies.

Non-Art Based Rejections

Figure 3 has been amended to add the legend "Prior Art" as requested. The applicant respectfully submits that the Figures satisfy the Examiner's objection.

With regard the formality objections the Examiner raised with regard to claims 1-5, the

applicant respectfully submits that new claims 32-36 address any perceived lack of clarity. Claim 13 has been amended to replace the semi-colon at the end of the preamble with a colon, as requested.

With regard to the Examiner's objections to claim 18, the applicant respectfully traverses the Examiner's objection. In the applicant's respectful submission, the quantities x and y used in the claim would be well understood by those of ordinary skill in the art to be dummy variables for use in the steps defined in the claim. Accordingly, the applicant respectfully submits that claim 18 complies with 35 U.S.C. § 112, second paragraph.

Cited Prior Art

The Irwin reference describes a two-stage method of translating an address. The first stage includes a 16-bit binary decoding tree stored in RAM (column 6, lines 38-64). The second stage is an associative search of network addresses stored in logical bins having a specific prefix value and encoded in a content addressable memory (CAM). A CAM is a device that operates in a manner opposite to the manner in which RAM is accessed. In a CAM, the input is a content and the output is a memory location where the content is stored in the CAM. (described in Irwin col. 6 lines 30-37).

The method described by Irwin contemplates a second stage having a single CAM using a binary search process. A binary search process compares entire search words. The CAM of the secondary stage stores a list of words.

The Hariguchi reference describes the internal structure of a CAM device. In particular, Hariguchi refers to the process of retrieving a single routing entry from the CAM (column 5, lines 50-55). The word "parallel" in column 5, line 53 refers to the internal operation of CAM cells, and not the CAM itself as a memory device. This internal parallel operation is not visible to the circuitry that uses the CAM as a memory device.

The Perlman reference describes a prefix address look-up system. Perlman describes a

router database containing a comparison table with a plurality of entries. As described at column 14, lines 10-20, the method described by Perlman contemplates performing successive parallel comparison operations to determine a result for one destination address. The loop repeats a process of fetching k padded addresses if the required output-port information is not found by circuitry 1250. As indicated in Figure 12 and within the disclosure in Perlman, the circuitry 1250 performs parallel comparisons between k padded prefixes and one destination address. Perlman describes two corresponding tables (680 and 690) where table 680 contains routing and forwarding information and table 690 contains next-address information.

The Examiner stated that Perlman disclosed a plurality of secondary search units including tables V and T and the steps of accessing table V indicated by the pointer using each successive remaining bit of the address in order, accessing table T at each successive location corresponding to the location of table V, and reading valid data contained at the location table T. The Examiner references columns 12 and 14 of the Perlman reference. The applicant respectfully submits that Perlman does not disclose a system using a primary and secondary search. Perlman describes a process of successive parallel comparison operations performed in a loop with regard to a single destination address. As Perlman notes in column 11, lines 20-25, the router database may include a routing and forwarding information table and a next address information table. The two tables described by Perlman bear no relation to tables V and T described in the present application. Tables V and T of the present invention are used to provide an efficient method of encoding several tree-branches to be stored in one of the secondary memory devices. Table V stores multi-threaded recursive pointers, each tracking one of the tree-branches. Table T stores the required translation. The method described by Perlman fails to disclose accessing table V at a pointer location obtained from the indexing table. Moreoever, Perlman fails to disclose a step of using each successive remaining bit of the address in order when accessing table V. Perlman also fails to disclose a step of accessing prefix data in table T at a location corresponding to the location accessed in table V. The Perlman reference describes a method of comparing a padded address with a number of padded prefixes. This is a process of comparing entire words, not bit-by-bit

navigation. There is nothing in Perlman to suggest a step of accessing a recursive-pointer table V of a search unit. This follows from the fact that the system described by Perlman has an entirely different foundation and follows an entirely different approach.

The Present Invention

The present invention is directed to a method and system for translating addresses in a telecommunication system. Within the application embodiments are disclosed that feature a two stage address translation process. In the first stage, a portion of the address is used to index a first table. The term "index" refers to a single access to a specified memory. By restricting the indexing to a sub-portion of the address of length A, the size of the memory for indexing is kept to a reasonable size while still providing for very fast indexing.

The result of the indexing is either a translation corresponding to a prefix or it is information leading to the second stage. The second stage of the present invention comprises a plurality of secondary search units. Each of the search units includes interleaved binary trees. The information obtained during the indexing stage either contains the translation or points to one of the secondary search units and points to a root of a particular binary tree within that secondary search unit. Accordingly, following the indexing step, a tree-search (also called a branch-search) process takes place beginning at the root indicated by the result of the indexing. By providing for multiple secondary search units and a plurality of interleaved binary tree structures in the second stage, the present invention accommodates multiple concurrent secondary searches for different addresses. Accordingly, the slower tree-search process of the secondary stage does not result in a bottle neck limiting the speed of address translation.

Art Based Rejections

In the Examiner's Report, the Examiner rejected claims 1-3 and 28 as being obvious having regard to US Patent No. 6,052,683 (Irwin) in view of US Patent No. 6,307,855 (Hariguchi). The Examiner also rejected claims 13-19 and 23-25 as being obvious having regard to

Irwin in view of US Patent No. 6,526,055 (Perlman). In addition to these rejections, the Examiner rejected the remaining dependent claims as being obvious having regard to various combinations of Irwin, Hariguchi, Perlman, US Patent No. 6,563,823 (Przygienda), and US Patent No. 5,909,440 (Ferguson).

The applicant has carefully considered the Examiner's art-based rejections, but respectfully traverses those rejections for the following reasons.

Claim 13 was rejected as being unpatentable over Irwin in view of Perlman.

Claim 13 is directed to a method of resolving addresses into prefixes including steps of indexing a table to generate a pointer to a secondary search unit, accessing a table V of the secondary search unit using successive remaining bits of the address, accessing table T of the secondary search unit, and reading valid data in table T at the location corresponding to the location accessed in table V, wherein the valid data indicates the prefix.

In rejecting claim 13, the Examiner asserted that Irwin disclosed a method of resolving addresses into prefixes using a length sorted table and a plurality of secondary search units, the method including a step of indexing the length sorted table using a portion of the address to create a prefix or pointer to a secondary search unit. As noted above, Irwin does not disclose a plurality of secondary search units. Irwin describes a single second stage CAM device for performing a binary search. The first stage of Irwin would not result in a pointer to a secondary search unit since Irwin describes a system having only one secondary memory.

The Examiner has suggested that Perlman discloses the remaining elements of claim 13. As noted-above, the Perlman reference fails to disclose the steps claimed in claim 13. Nothing in the Perlman reference points to a table having interleaved or recursive pointers and a corresponding table containing the resulting prefix corresponding to locations in the first table, wherein the first table is navigated using successive remaining bits of the

address. Accordingly, in the applicant's respectful submission, claim 13 of the present application is not obvious in view of Irwin or Perlman, alone or in combination.

Regarding the Examiner's assertion that it would be obvious to modify the teachings of Irwin to include the features of the present invention in view of Perlman, the applicant respectfully notes that neither of the references teach the steps claimed in claim 13 of the present application. Therefore, even if one were to combine the teachings of Irwin and Perlman, one does not arrive at the invention defined in claim 13. Moreover, one skilled in the art would not be inclined to modify the teachings of Irwin to provide for a plurality of secondary search units having interleaved recursive pointers, since Irwin teaches the use of a content addressable memory (CAM), which operates on an entirely different principle.

Claim 23 was rejected as being obvious having regard to Irwin in view of Perlman.

The applicant's submissions above in relation to claim 13 are repeated with regard to claim 23.

Claim 23 is directed to an apparatus for address translation that includes an indexing block for directly accessing a sorted prefix directory to obtain data specifying one of a plurality of secondary search units based upon the first A binary bits of the address, and a plurality of secondary search units having tables V and T containing interleaved tree branches and providing translated prefixes.

The cited passage in Irwin (column 6, lines 38-55), describes the first stage selection of an address as being subject to a search algorithm in look-up table module 66. Moreover, Irwin does disclose obtaining data specifying one of a plurality of secondary search units, since Irwin contemplates only a single secondary memory (the CAM).

The Examiner states that Perlman discloses a plurality of secondary search units for searching in parallel through a secondary memory specified by the indexing block for prefixes of length and longer than A. Column 12, lines 5-20 is referenced. It is respectfully

submitted that there is no indexing block in the system taught by Perlman and, further, there is no parallel processing of addresses. Column 12, lines 5 to 20 of Perlman describe the process of comparing one address with several padded prefixes. Multiple addresses are not processed at once.

The Examiner also states that the Perlman reference teaches secondary memories comprising table V and T. As described above, tables 680 and 690 containing routing and forwarding information and next address information cannot be equated to tables V and T of the present invention. The tables described by Perlman do not contain interleaved tree branches and they do not provide translated prefixes at a location corresponding to the location accessed in the other table. Accordingly, Perlman fails to teach or suggest the features claimed in claim 23 of the present invention.

The Examiner states that it would have been obvious to modify the teachings of Irwin to include a memory storing two tables for each search unit on the basis of the teachings in Perlman. In the applicant's respectful submission, both references fail to teach the features claimed in claim 23 of the present invention. Accordingly, even if one combines the teachings of the two references one does not arrive at the invention defined in the claim 23. Moreover, one of ordinary skill in the art would not be inclined to modify Irwin to provide for a plurality of secondary search units, each having tables with interleaved branches for tree-searching, since Irwin teaches away from this concept by advocating the use of a single CAM performing a binary search.

Claim 28 was rejected as being obvious having regard to Irwin in view of Hariguchi.

Claim 28 is directed to an address translation apparatus including a primary translation unit containing a primary translation table having locations of branch search data structures in secondary search units, and a plurality of secondary search units for performing secondary searches in parallel, each secondary search unit having the branch search data structure for performing a secondary search and translating an address to a prefix, where the primary translation table indicates the location of the branch search data structure for

beginning the secondary search.

The submissions provided with respect to claims 13 and 23 are repeated and relied upon in connection with claim 28.

The Examiner states that Irwin discloses a primary translation unit and a plurality of secondary search units. As noted above, the applicant respectfully submits that Irwin does not disclose a primary translation unit providing locations of branch search data structures and secondary search units. Irwin describes only a single secondary CAM performing a binary searching. The CAM does not include branch search data structures. Accordingly, Irwin neither teaches nor suggests providing a table that contains locations of branch search data structures.

Irwin also does not teach or suggest a plurality of secondary search units. Irwin teaches only a single CAM performing a binary search. Irwin also fails to teach or suggest the secondary units having branch search data structures. Irwin contemplates only a binary search in the CAM. By teaching the use of a CAM, Irwin teaches away from the concept of a plurality of interleaved branch searches.

The Hariguchi reference also only describes a single CAM device. Hariguchi describes the internal operation of the CAM device. Hariguchi teaches a process of retrieving a single routing entry from the CAM. Hariguchi fails to teach or suggest performing secondary searches in parallel, as suggested by the Examiner.

Therefore, the applicant respectfully submits that neither reference, alone or in combination, teaches or suggests the invention claimed in claim 28 of the present application. If one were to combine the teachings of Irwin with the teachings of Hariguchi, one does not arrive at the invention defined in claim 28. Moreover, it would not have been obvious to a person of ordinary skill in the art to modify the teachings of Irwin in view of Hariguchi to arrive at the apparatus claimed in claim 28 of the present invention, for all of the foregoing reasons.

Dependent Claims

In rejecting some of the dependent claims, the Examiner relied upon Przygienda, stating that Przygienda disclosed a step of scrambling an address according to a predetermined reproducible formula (column 7, lines 45-60). In the applicant's respectful submission, Przygienda fails to teach or disclose a step of scrambling an address. Nothing is mentioned in the referenced passage regarding the scrambling of an address in the context of address translation.

Summary

In view of the foregoing submissions, the applicant respectfully traverses the Examiner's rejection of claims 13, 23, and 28 and submits that these claims are patentably distinguishable over any combination of Irwin, Perlman, or Hariguchi. For substantially the same reasons, the applicant respectfully submits that dependent claims 14-22, 24-27, and 29-31 are also patentably distinguishable over the cited references.

New claim 32 is directed to a method having steps of indexing to obtain a translation code and a pair of pointers, and accessing a secondary memory device to perform a tree-search process at a root defined by one of the pointers. The applicant respectfully submits that new claims 32 through 36 are also patentably distinguishable over the cited references.

In view of the foregoing amendments and submissions, the applicant respectfully requests that the Examiner withdraw his art-based rejection and requests that a timely

Notice of Allowance be issued. Should the Examiner have any questions with respect to these submissions, please contact Fraser Rowand at (416) 868-1482.

Respectfully Submitted,
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